# A 2-32 GHz Coplanar Waveguide InAlAs/InGaAs-InP HBT Cascode Distributed Amplifier

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**Abstract**

A 2-32 GHz InAlAs/InGaAs-InP HBT CPW distributed amplifier (DA) has been demonstrated which benchmarks the highest bandwidth reported for an HBT DA. The DA combines a 100 GHz $f_{max}$ and 60 GHz $f_T$ HBT technology with a cascode coplanar waveguide DA topology to achieve this record bandwidth. The cascode CPW DA demonstrates both design techniques and technology capability which can be applied to more complex circuit functions such as active baluns for mixers, active combiners/dividers, and low dc power-broadband amplification at millimeter-wave frequencies.

## I. Introduction

Previously reported HBT distributed amplifier gain and bandwidth performance are summarized in Fig. 1 [1],[2],[3],[4]. The 2-32 GHz response of the present work is believed to be the highest bandwidth reported for an HBT distributed amplifier, and is also the first CPW DA design implemented in InAlAs/InGaAs-InP HBT technology. A 33 GHz InAlAs/InGaAs-based HBT cascode direct-coupled amplifier has also been previously reported[5]. However, due to the use of an unmatched analog design topology, the return-loss was < 5 dB for frequencies > 16 GHz which, unfortunately, limits the practical bandwidth to less than half of the amplifier's 3-dB bandwidth. The present work achieves good broadband return-loss which is typically > 13 dB across the full band using a distributively matched topology.

## II. InAlAs/InGaAs HBT Technology

A similar 1-μm fully self-aligned InAlAs/InGaAs HBT process has previously been described in detail[6] along with several MMIC demonstrations [7],[8],[9],[10],[11]. The InAlAs/InGaAs HBT device structures are grown using solid source Molecular Beam Epitaxy. Be and Si are used as p- and n-type dopants for the base and emitter/collector,

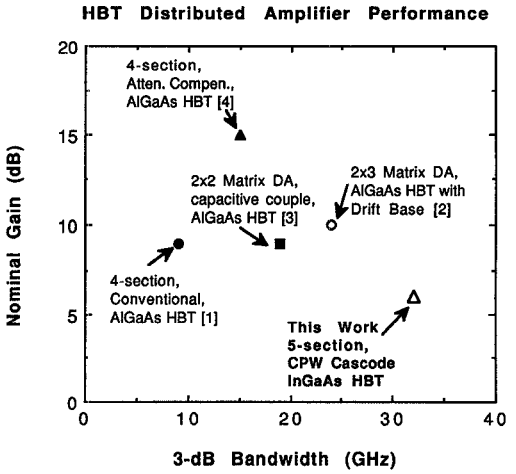


Fig. 1 Summary of previously reported HBT DA gain and bandwidth performance: Nominal Gain vs. 3-dB Bandwidth.

respectively. The base-collector epitaxial structure consists of a base thickness of 800 Å uniformly doped to $3x10^{19}$ $cm^{-3}$, a 7000Å thick n-type collector lightly doped to $1x10^{16}$ $cm^{-3}$, and an $N^+$ sub-collector doped to $2x10^{19}$ $cm^{-3}$. The emitter structure incorporates an InGaAs/InAlAs cap which is heavily doped for good emitter contact. The base-emitter junction consists of a compositionally graded quarternary layer of $In_{1-x-y}$ $Ga_x$ $Al_y$ As. Compositional base-emitter grading is used to achieve uniformly consistent dc beta and $V_{be}$ matching between devices, as well as for producing consistently repeatable device rf performance. The HBT dc beta across the wafers are typically 20 at a Jc=10 $kA/cm^2$. The breakdown voltage $BV_{ceo}$ is ≈11V and the $BV_{cbo}$ is ≈13 V.

A high performance fully self-aligned 1-μm emitter width process is used to produce HBTs with an $f_T$ and $f_{max}$(from MAG) of ≈ 60 and 100 GHz, respectively. The corresponding device $f_{umax}$ (from unilateral gain) is 130 GHz. These numbers were achieved from a 1x10 $\mu m^2$ quad-emitter HBT biased at a current density of Jc=120 $kA/cm^2$ and a Vce= 2.0V.





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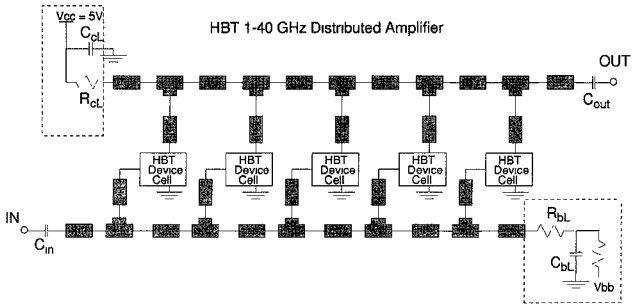


Fig. 2 Design topology of the 5-section CPW HBT cascode DA.

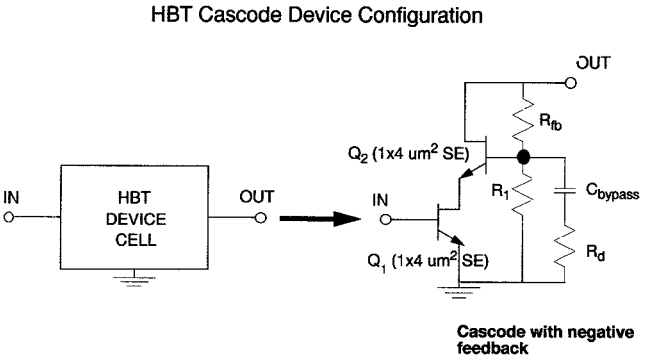


Fig. 3 HBT cascode gain cell.

### III. CPW HBT Cascode Design

Fig. 2 shows the design topology of the 5-section CPW HBT cascode DA. A CPW design environment was used because it offers smaller chip size implementation, lower parasitic ground inductance, and easier manufacturability because backside vias are not required. In addition, a CPW design environment can minimize interline coupling between transmission lines and proximity effects which simplifies the circuit modeling at millimeter-wave. This last advantage is especially attractive for millimeter-wave HBT DAs because the small inductive line lengths normally required to construct a distributive network with the HBT's high input capacitance, are sensitive to the close proximity of backside vias and other microstrip components. Also, the high conductor loss characteristic of CPW does not significantly impact the HBT DA design because the losses of the HBT device usually dominate the loss of the distributed transmission-line network[4].

A cascode HBT gain cell is used as a high wideband gain block in the distributed amplifier design. The schematic of the HBT cascode gain cell which is used in each section of the DA is given in Fig. 3. A common-emitter transistor, $Q_1$, is connected to a common-base transistor, $Q_2$, to form a cascode pair. Both Q1 and Q2 are 1x4 $\mu m^2$ single-emitter HBTs nominally biased at an $I_C$= 2 mA and a $V_{ce} \approx$ 1.7V. Fig. 4 shows the transistors $f_T$ and $f_{max}$ performance plotted versus collector current. This device size was able to achieve a peak $f_T$ and $f_{max}$ of 46 GHz and 84 GHz, respectively. The size of the HBT device and operating current was chosen from a compromise between the available gain and input capacitance of the device. At the chosen design operating current of 2 mA, the HBTs have an effective input capacitance of $\approx$ 0.5 pF and an $f_{max} \approx$ 75 GHz. In the cascode topology of figure 3, the base of transistor $Q_2$ is biased through a voltage divider provided by resistors $R_1$ and $R_{fb}$. The base of $Q_2$ is also ac bypassed by a series R-C network consisting of $C_{bypass}$ and $R_d$. The cascode

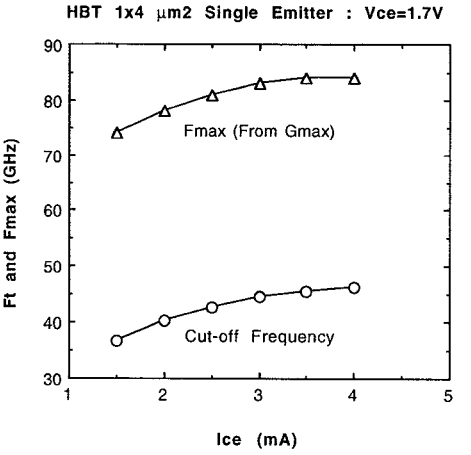


Fig. 4 $f_T$ and $f_{max}$ versus Ic for a 1x4 $\mu m^2$ HBT device.

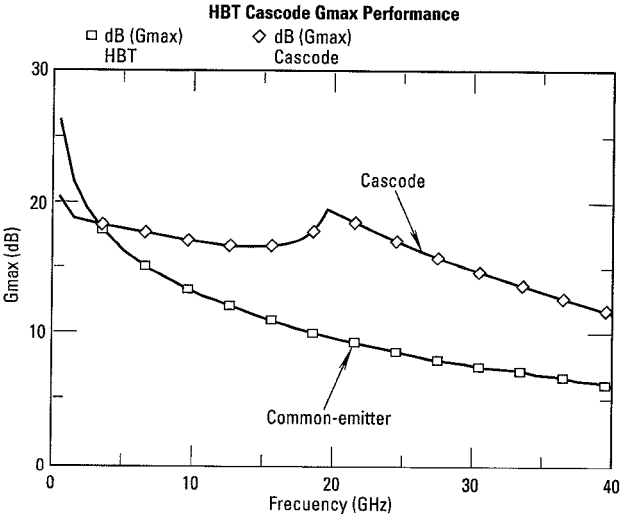


Fig. 5 $G_{max}$ performance of the cascode cell compared to a conventional common-emitter HBT.

cell employs negative feedback through resistors $R_{fb}$ and finite resistance $R_d$ in order to maintain unconditional amplifier stability. Fig. 5 illustrates the superior $G_{max}$ performance of the HBT cascode cell compared to a conventional common-emitter HBT. At frequencies above 20

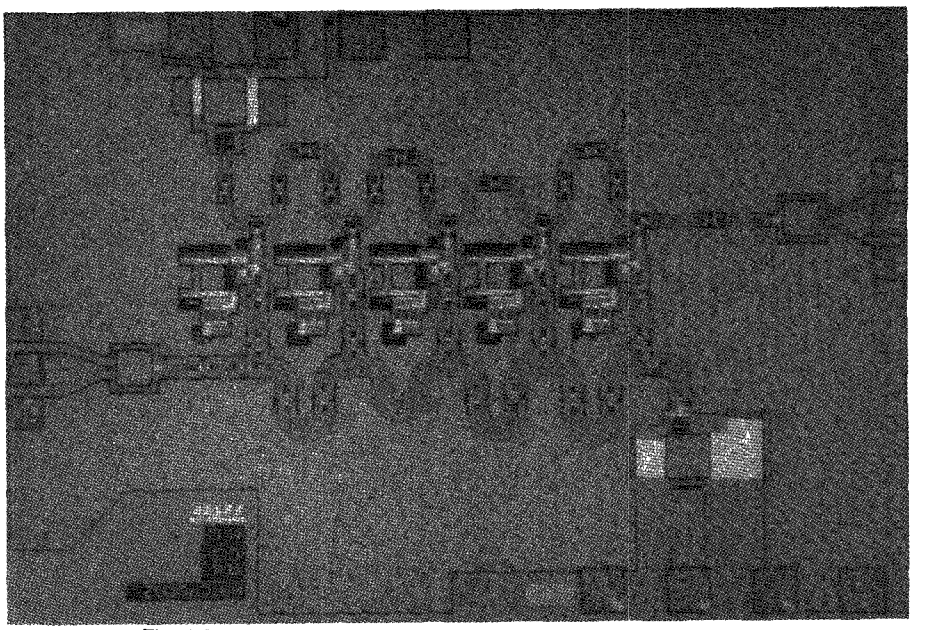

Fig. 6 Microphotograph of the fabricated CPW cascode HBT DA. Chip size is 1.3x1.2 $mm^2$.

GHz, the cascode offers as much as *7 dB more available device gain*. The amplifier supply voltage is 5V and draws 33 mA of current. The total power consumption is 165 mW. Fig. 6 shows a microphotograph of the fabricated CPW cascode HBT. This photograph illustrates how compact the transmission line networks are about each of the 5 HBT cascode gain cells. Had a microstrip environment been used, backside vias would have been required for each of the cascode cells and would have made the input and output transmission-line networks almost physically impossible to layout. The microstrip design would have degraded the performance because of its sensitivity to proximity effects, whereas, the CPW design geometrically confines the fields such that the proximity effects of adjacent structures are lessened. Recently reported experimental data supporting this claim demonstrated that as much as a 10 dB improvement in isolation between arms of a SPDT switch at millimeter-wave frequencies can be achieved using a CPW environment[12]. Thus, our CPW DA approach allows the design to be more easily modeled and results in a compact chip area of 1.8x1.2 $mm^2$.

## IV. Measured Results

The original simulation performance of the HBT cascode CPW DA is compared against the measured performance as shown in Fig. 7. A 5 dB gain and 40 GHz 3-dB bandwidth was predicted while a 5.5-6 dB gain and 32 GHz bandwidth was measured. The measured return-losses are better than 13 dB across most of the 2-40 GHz band. The discrepancy between the original simulation and measured data is due to a difference in performance between the HBT design model and the actual fabricated devices. Because a cascode pair is used for the gain cell, even a slight change in performance in the HBTs could result in a dramatic change in the amplifier's bandwidth response. When a new HBT design model is generated from the more recent device s-parameters (taken from the same site/wafer as the measured circuit data) and used in the simulation, the distributed amplifier's simulated gain matches

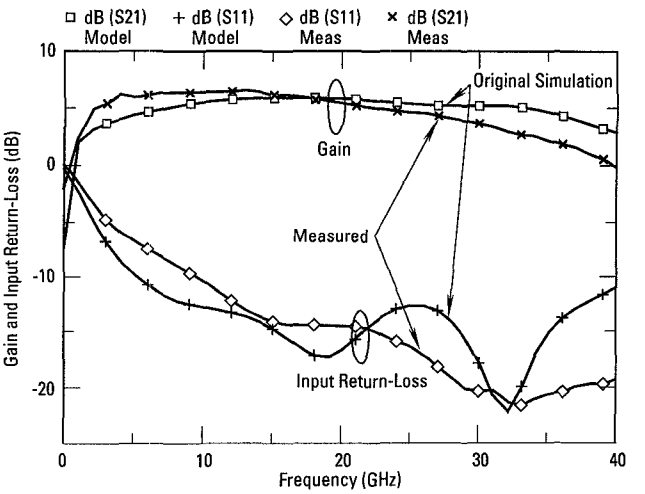


Fig. 7 Original simulation versus the measured performance.

its measured gain to within 0.5 dB up to 40 GHz, shown in Fig. 8. The corresponding modeled input return-loss also closely matches the measured data. For frequencies above 20 GHz, the input return-loss actually becomes much better than the modeled by > 5 dB. Fig. 9 also illustrates that the modeled output return-loss tracks the measured data which is better than 15 dB across most of the band. Even the simulated resonances in the output return-loss response match the measured response to within a few GHz. Both Figs. 8 and 9 seem to reflect the accuracy of the LIBRA(4.0) CPW models when the circuit is layed-out to minimize proximity, radiation, and parasitic effects.

## V. Conclusion

We have demonstrated a 2-32 GHz HBT distributed amplifier which is believed to be the highest reported bandwidth for an HBT DA. A 5-section cascode DA topology based on an InAlAs/InGaAs-InP HBT technology was used to achieve this benchmark. A CPW design environment was implemented in order to minimize interline coupling and proximity effects as well as to simplify the DA's fabrication. The cascode HBT CPW DA demonstrates both design techniques and technology capability which can be applied to other millimeter-wave MMIC circuit functions such as active baluns for mixers, active combiners/dividers, and low dc power-broadband amplification at millimeter-wave frequencies.


## Acknowledgments

The authors would like to acknowledge K. Minot and J. Lester for their advise on CPW design and layout, T. Naeole for wafer processing, and W. Bartolome for layout support.


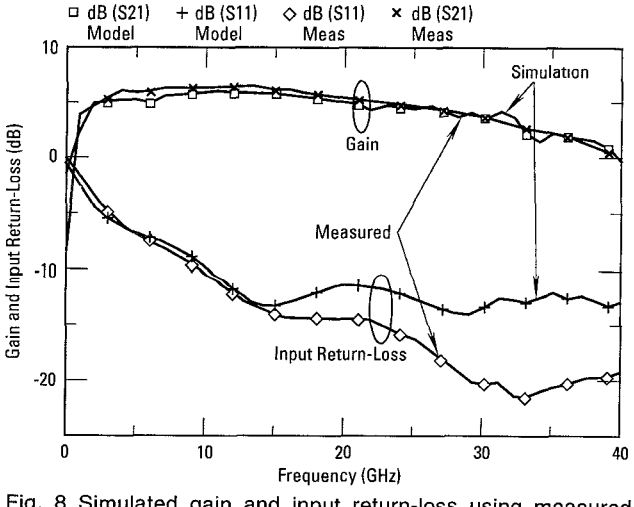


Fig. 8 Simulated gain and input return-loss using measured HBT s-parameters (from same wafer-site as the measured circuit) vs. measured circuit performance.

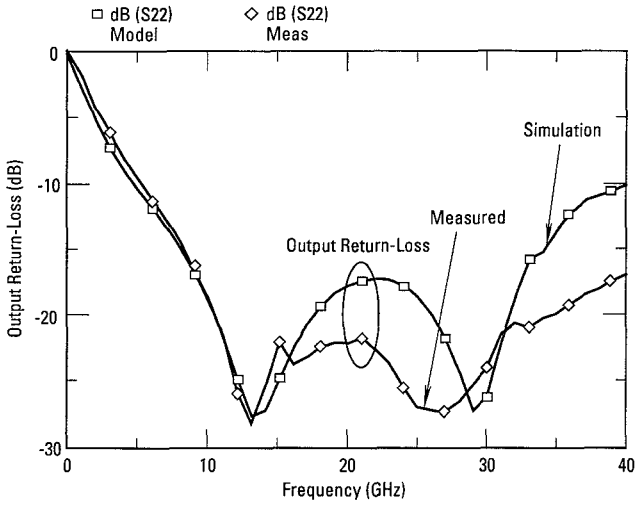


Fig. 9 Simulated output return-loss using measured HBT s-parameters (from same wafer-site as the measured circuit) vs. measured circuit performance.

## References


[1] B. Nelson, et.al., "High Linearity, low dc power monolithic GaAs HBT broadband amplifiers to 11 GHz", in *1990 IEEE Microwave and Millimeter-Wave Monolithic Circuit Symp. Dig.*, Dallas, TX, pp. 15-18.

[2] K.W. Kobayashi, et.al., "GaAs HBT wideband matrix distributed and Darlington feedback amplifiers to 24 GHz", *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 12, pp. 2001-2009, Dec., 1991.

[3] K.W. Chang, et.al., "2-19-GHz Low Power and High-IP3 Monolithic HBT Matrix Amplifier", *IEEE Microwave Guided Wave Lett.*, vol. 2, pp. 17-19, Jan. 1992.

[4] K.W. Kobayashi, et.al., "A Novel HBT Distributed Amplifier Design Topology based on Attenuation Compensation Techniques", 1994 *IEEE Microwave and Millimeter-Wave Monolithic Circuit Symp. Dig.*, San Diego, CA, pp. 179-182.

[5] M. Rodwell, et.al., "33 GHz Monolithic Cascode AlInAs/GaInAs Heterojunction Bipolar Transistor Feedback Amplifier," in *IEEE 1990 BCTM Dig.*, pp. 252-255.

[6] L.T. Tran, et.al., "InAlAs/InGaAs HBT with Exponentially Graded Base Doping and Graded InGaAlAs Emitter-Base Junction," in *1992 IEEE Indium Phosphide and Related Materials Dig.*, Newport, Rhode Island, 1992, pp. 439-441.

[7] K.W. Kobayashi, et.al., "InP based HBT Millimeter-Wave Technology and Circuit performance to 40 GHz," in *1993 IEEE MMWMC Symp. Dig.*, Atlanta, Georgia, pp.85-88.

[8] K.W. Kobayashi, et.al., "A Novel Active Feedback Design Using InAlAs/InGaAs Heterojunction Bipolar Transistors," in *IEEE Microwave and Guided-Wave Letts.*, vol. 4, no. 5, pp.146-148, May 1994.

[9] K.W. Kobayashi and A.K. Oki, "A Novel Heterojunction Bipolar Transistor VCO using an Active Tuneable Inductance," *IEEE Microwave and Guided-Wave Letts.*, vol. 4, no. 7, 1994.

[10] K.W. Kobayashi, et.al., "Low Power Consumption InAlAs/InGaAs-As/InGaAs HBT X-band Double-Balanced Upconverter," in *IEEE IEEE Trans. on JSSC*, vol. 29, no. 10, Oct., 1994, pp. 1238-1243.

[11] K.W. Kobayashi, et.al., "Low Power Consumption InAlAs/InGaAs-InP HBT X-band SPDT PIN Diode Switch," in *IEEE Microwave and Guided-Wave Lett.*, vol. 10. no. 3.

[12] K.W. Kobayashi, et.al., "A 50 MHz-30 GHz Broadband Co-Planar Waveguide SPDT PIN Diode Switch with 45 dB Isolaion," *IEEE Microwave & Guided-Wave Letts.*, vol. 5, no. 2, 1994.